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Keynote Speech

In the real world, most of the data is characterized by analog signals. In order to process the data using a microprocessor, we need to convert the analog signals to the digital signals, so that the microprocessor will be able to read, understand and process the data.

I will present the research conducted on a power efficient 5-bit parallel comparator analogue to digital converter. The block diagram of the converter is represented by two schematic blocks, one comparator and the other digital encoder. In this operation, the speed of the encoder is increased with the exertion of the encoder through the organization of modified differential cascade voltage switch logic. The purpose of the aforesaid encoder is attributed to the translation of thermometer code to Gray code and to restrain minimum probability of bubble errors and meta-stability in the circuit. The 5-bit parallel comparator analogue to digital converter is designed using 180 nm CMOS technology at a supply voltage of ± 0.85 V.

The projected flash ADC is highly linear with worst-case differential non-linearity of -0.35 LSB and integral non-linearity of -0.28 LSB. The computed power dissipation is of 23.29 mW. The circuit so designed and proposed has wider applications, especially in several communication systems, instrumentation, applied electronics and signal processing units etc.