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Title of the Keynote Address: **"Effort Delay and Appropriate Optimizing Techniques"**

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## ABSTRACT

Accurate delay estimation and design of delay equalizers have of late become important in low-power, low-voltage processor design, optimization, multicore processors and signal processing applications such as delay equalized chains, wave pipe-lining, velocity selective recording of ENG and other biomedical signals. This is further significant because still most of the chain-of-delay blocks in analogue, mixed-mode and biomedical systems are pre-processed by manual designing prior to computerized/ digital post processing.

A chain of logic gates can be cleverly designed to realize delay accurately. Likewise optimum delay in circuits is observed to be realizable by appropriate selection of the topology and the device dimensions. The present endeavor is to analyze different types of delays – both topology dependent and topology independent and suggest optimum design methodology in a systematic study.

The lecture proposes to cover a wide range of circuit design techniques from examples where a systematic method can be used (instead of trial-and-error) to arrive at the best topology and transistor dimensions for optimum delay. The delay chain with branching shall also be taken into account through examples and the best topology and dimension for delay-optimization for network with branching shall also be proposed. Traditionally, string-of-inverters with geometrically increasing sizes

were used to drive large capacitive loads. Sizes were arbitrarily decided and optimized by designers of semi- custom and full-custom devices. Subsequently different optimization techniques were evolved that used El-More's concept of sizing of chain of delays and were further optimized by circuit designers thereafter. Although parasitic delay is intrinsic to a design, it can still be optimized as it was observed by clever design of fan-out.

Similarly, the effort delay, which was dependent on the topology, could also be optimized keeping the functionality as before. This included appropriate choice of topology and optimum sizing of the devices in the chosen topology. There have been many techniques to this end available in open literature. However the topic and coverage of this presentation has its genesis in the pioneering work on logical effort, electrical effort and branching effort in estimating effort delay by Ivan Sutherland et al, brought out in "Logical Effort: Designing Fast CMOS Circuits" Morgan-Kaufmann Publishers and studies by subsequent authors to this end. However appropriate circuit examples and techniques for solving design exercise with exceptions therein have been added to enrich the theory.

The ideal target-audience include participants of the conference, members of the scientific community apart from young researchers working on circuits for low power, low voltage processor, digital-core, mixed-mode, analogue and biomedical system designers.

The duration shall be about 1-hour depending including interactions.